Bitscope Enhanced Firmware (BC000120 - DRAFT)

The existing Bitscope PIC (BC000112) is a 16F84 device with 1K words of program memory and 68 bytes of RAM. This PIC is limited in functionality mainly by the program memory size and to some extent by the available RAM.

Microchip now have several 18 pin PIC devices which are plug compatible with the 16F84. These PICS have 2K of program memory and run at 20MHz (115kB/5mips). The extra 1K of program can be used to impliment new modes to increase the functionality of Bitscope with a simple chip replacement. Also, the new chips have over 128 bytes of RAM allowing new VMR parameters for new functional modes.

The new chip will be available as a chip or on a PCB header with a 20MHz XTAL on board so existing Bitscopes will not need in-field board level mods, apart from a socketed chip replacement. New Bitscopes can get the 20MHz chip and XTAL as standard.

The current BC000112 code will remain in place in the new revision without modification to ensure all existing software will work with the new chip.

Limitations of BC000112

The main problems with BC000112 which have become apparent are as follows:-

- Download speed of 57K6 baud is slow
- Lack of sample rates between 200K and 25M
- Difficult calculations for Post Trigger delay
- Missing Trigger data for long PTD captures
- Accurate location of trigger events
- Frequency determination for noisy analog signals
- False Triggering due to ADC noise
- Limited Slow Clock Logic Capture modes
- Inability to differentiate PIC devices from different Software Vendors

Enhancements to BC000112

With the new 2K PIC devices from MicroChip, we have been able to address these problems while leaving all the current BC000112 code intact. This means the new PIC will work in current configurations, and new software can "turn on" features as required. By allowing a Vendor string to be programmed into BC000120, specialised applications can key advanced features to a PIC sold with the software. This does not disable any functionality in the PIC, but does allow a third party software vendor to target his user base.

We have also provided a Serial number facility where each PIC may be programmed with a unique number in code for special software licencing purposes. This will not be standard, but can be an option at Program Time.

A further enhancement will be available using MicroChip's new 16F628 Flash part. This device has an onboard HW UART which can operate to over 1Mb/s. Using this HW UART requires a special carrier to activate the correct pins. This chip will allow 2 significant improvements to Bitscope -

1. Moving the UART into HW means the PIC can be executing (some) ByteCode instructions while the next one is being assembled in the UART. Most of the data entry ByteCodes execute in a few uS, so that means that the protocol can be changed so the Host can transmit a whole string to Bitscope and handshake the whole string instead of byte by byte. This should greatly speed up RT operation without having to write a special threaded serial handler. An example of a script that can be sent to Bitscope 'whole' is :-

   [03]@[00]sn[10]s[21]@[03]sn[00]sn[01]sn[02]sn[03]s

   This example string can be sent to bitscope and deemed complete when the whole string is received back, since each ByteCode command is guaranteed to execute in less than 1 serial character time.

   The Host will be able to identify a HW UART Bitscope by the BC number. All other functionality will be identical to the non-HW UART PIC.

2. Speeding up the serial connection allows us to provide USB support for existing Bitscopes by building a custom USB <->Bitscope plug. This plug can accelerate the Bitscope to 1Mb/s with only a PIC upgrade, protecting the current bitscope owners from USB induced obsolecence.

Baud Rate increase

By running the PIC at 20MHz, the software timed UART will automatically run at 115K Baud. This applies to the current BC000112 in 16F84A devices, and has been shown to work.

Binary dump mode (A)nalog command

This command currently dumps up to 256 bytes of analog sample RAM in a binary format. By adding a mode register, data transfer efficiency is improved and new features are added - Software TimeBase and Variable Aperture Processing. This command gets four new VM registers - a mode register, two parameter registers and a count register.

A_MODE,

SEND,
SKIP,
REPEAT

The new modes are as follows: -

A-Mode 0
Implements the default (A) command and is selected on power up for compatability.

A-Mode 1 - Software TimeBase
This mode uses two new parameter registers - SEND and SKIP. This will dump (SEND) bytes from analog RAM then advance by (SKIP) addresses. The REPEAT register will control how many of the above cycles are performed.

If (SEND) is greater than 1, then we will get a dump of (SEND) bytes of data separated by (SKIP) addresses. The groups of data may be used by the host to indicate HF noise or alternately, a waveform may be displayed progressively using data scattered across all of sample RAM as opposed to sequentially. This mode also allows interleaved channel data to be extracted before it is sent to the host.

'A'mode-1 allows samples at selected intervals in sample RAM to be dumped to the host by specifying a (SKIP) value of 1 to 255. This is a firmware version of the enhanced Trace modes, although subject to RAM limits of 16K sample, total capture time is not improved. By dumping 1 byte, then skipping 0-255, it is possible to implement a software Sample Rate of 25MHz/n where n= 1,256.This takes us down to 100KHz where we can retrieve 64 samples from RAM. If n=5, we effectively have a 5MHz sample rate and can dump 3,200 samples from memory.

A-Mode 2 - Variable Aperture
This mode also uses the two new parameter registers - SEND and SKIP. This mode will cause (SEND) contiguous bytes in analog RAM to be converted into signed 16 bit integers and summed to a 16 bit result. This 16 bit signed integer sum will be transmitted to the host. Following this operation (SKIP) bytes in analog RAM will be ignored. This cycle is repeated according to the value in the (REPEAT) register. Since the maximum number of summed 8 bit values is 256, the result can always be represented as a 16 bit signed int.

This mode also effects a variable sample rate by varying the intervals in sample RAM between data transmitted to the host. In addition (SEND) samples are effectively summed or averaged. This is like varying the aperture of the AD convertor. If (SEND)=16 then the sample value sent to

the host is the aggregate of sampled values over 16 ADC clock cycles. This sum has a possible 4096 values - equivalent to a 12 bit number - allowing greater ADC precision. In addition, the signal BW has been divided by 16. This mode provides a very efficient way to synthesize TimeBase modes between 100KHz and 25 MHz while still using all the ADC data we have recorded. The averaging of many samples will decimate any HF components in the signal removing the possibilities of aliasing. This will not prevent aliasing from components above Nyquist rate, however. The limitation on this mode is the period that may be sampled in a 16K block of available sample RAM at the selected sample rate.

A further consideration of using Variable Aperture mode is that the Host must account for the scaling factor introduced by the summing of (SEND)samples. In the example where (SEND) is 16, Full Scale values sent to the host will be -2048/+2047. Host software must convert this to the real voltage range of the input channel. In the extreme case where 256 samples are summed, the result is effectively a 16 bit ADC with values of -32768/+32767.

A-Mode 3 - Variable aperture with MIN-MAX
This mode is a variation of Mode 2, with the modification of computing the MIN and MAX values over the SEND range of captured samples. These values are transmited as (unsigned chars) instead of the 16 bit aggregate value. The host may use these values to display a more accurate image which will indicate the presence of a HF component on the decimated average signal. Again, the number of data sets (2 bytes also in this case - MIN, MAX) is determined by the value in REPEAT. Since the set up values are the same for Mode-2 and Mode-3, both dump modes can be used on the same capture by simply changing the A-MODE, restarting SPOCK, then re-issueing the dump command.

Trigger (E)vent Scan command

This new command is designed to help locate trigger points in sample memory prior to a dump command. A section of sample RAM is searched from the current location in SPOCK, and either FALSE->TRUE transitions or TRUE->FALSE transitions are transmitted to the host as an ascii 16 bit address pointer with a CR to signify termination. If the trigger condition was not found, no address wil be transmitted, just a CR. A related operation is searching for whole waveforms in a captured block of data. This can be used to determine frequency

The Trigger event may be specified as Logical or Analog -

Logical - where the Trigger logic in SPOCK is used to assign a 0 or 1 to every sample as detailed in the Trigger Specification of the Programmers

Manual

Analog - where each analog sample is compared to a reference and TRUE represents GTE, FALSE represent LT.

(E) command has 5 new virtual registers :-
E_ MODE,
ECOUNT_HI,
ECOUNT_LO,
ELVL1,
ELVL2

E-Mode 0 - Positive Transition Logical Event
Uses SPOCK logic as set up for TRIGGER event to look for 0->1 transitions. The address of the '1' is transmitted as 4 ascii characters - 'a' 'a' 'a' 'a' with a <CR> being transmitted at END.

E-Mode 1 - Positive Transition Analog Event
Scans through the Analog Sample RAM from current location for up to ECOUNT locations looking for a transition from <sample(n)> LT <ELVL1> to <sample(n+1)> GTE <ELV1L>. The address of the sample (n+1) is transmitted as 4 ascii characters - 'a' 'a' 'a' 'a' with a <CR> being transmitted to terminate.

E-Mode 2 - Negative Transition Logical Event
Uses SPOCK logic as set up for TRIGGER event to look for 1->0 transitions. The address of the '1' is transmitted as 4 ascii characters 'a' 'a' 'a' 'a' with a <CR> being transmitted at END.

E-Mode 3 - Negative Transition Analog Event
Scans through the Analog Sample RAM from current location for up to ECOUNT locations looking for a transition from <sample(n)> GTE <ELVL2> to <sample(n+1)> LT <ELVL2>. The address of the sample (n+1) is transmitted as 4 ascii characters - 'a' 'a' 'a' 'a' with a <CR> being transmitted to terminate.

E-Mode 4 - Count logical cycles in address span
Scans through Sample RAM from current position looking for a positive transition on the SPOCK Trigger hardware -
T(n)FALSE -> T(n+1)TRUE
T(n+1) address is the beginning of the period counter

Scans through SAMPLE RAM from positive transition looking for a negative transition -
T(p)TRUE -> T(p+1)FALSE
Scans through SAMPLE RAM from negative transition looking for a

positive transition -
T(q)FALSE -> T(q+1)TRUE
T(q+1) is saved as the end of the period counter, cycle count is incremented

The sequence is repeated until ECOUNT is reached, then the number of whole cycles and the period of those is printed as comma separated ascii chars followed by a CR -

E
34,0c46

E-Mode 5 - Count analog cycles in address span with hysteresis
Scans through Analog RAM from current position looking for a positive transition -
A(n)<ELVL1 -> A(n+1) >=ELVL1
A(n+1) address is the beginning of the period counter

Scans through Analog RAM from positive transition looking for a negative transition -
A(p)>=ELVL2 -> A(p+1)<ELVL2
Scans through Analog RAM from negative transition looking for a positive transition -
A(q)<LVL1 -> A(q+1) >=LVL1
A(q+1) is saved as the end of the period counter, cycle count is incremented

The sequence is repeated until ECOUNT is reached, then the number of whole cycles and the period of those is printed as comma separated ascii chars followed by a CR -

E
04,13fe

The ELVL1 and ELVL2 parameters implement a hysteresis band to remove noise triggering. By varying these it is possible to extract the fundamental frequency of a periodic signal, where it is the dominant component. For very noisy signals analysis by FFT may be necessary.

Applications

This new mode avoids the need to use software in the host to accurately locate trigger points. The trigger point associated with (T)race modes has about 1uS of uncertainty. Using this new (E)vent mode, the trigger point can be accurately determined to the sample, and subsequently only the relevant sample data required can be dumped to to the host and displayed directly. This will allow a jitter free trace

using simple host software. Alternatively, if sample RAM is full of data, (E)vent command may be used to locate a small segment of data that contains a known number of whole waveforms, thus reducing the download time for the host.

The analog mode of (E)vent allows true level detection of trigger points in sample RAM - which is more versatile than the 0/1/X logic condition used with SPOCK trigger.

If (E) is used to locate zero crossings in a repeating waveform, this information can be used to determine the frequency without dumping the whole waveform to the host. This technique can be used to quickly identify the fundamental frequency of a waveform, or to automatically set the display parameters so a whole waveform is displayed.

Mode 4,5 go further by scanning a region of Sample RAM and determining the number of whole cycles and the period in sample clocks. Mode 5 uses hysteresis to reduce the effects of a noisy signal. In Signal Processing this is known as "Center Clipping". An upper and lower value are specified which operates like a Schmidt Trigger device - a positive edge must be greater than the high value, while a negative edge must be lower than the low value. Mode 5 can very simply allow the measurement of frequency up to 12.5MHz (Fs/2) by returning the period P of N samples.

For a 25MHz sample clock -

Freq = N/(P*0.04uS)MHz

The accuracy is determined by the period over which the measurement is made. If, say we measure N cycles over 10,000 sample clocks, the best accuracy possible is 1/10,000 - 100ppm. To do better, we must average over a number of captures which will provide a result converging on the accuracy of the Bitscope sample OSCILLATOR device.

(D)elayed Mode Trace command

This is a new Trace mode command that is especially effective for DSO analog captures, although it may also be used for Digital and mixed mode captures. This mode always triggers at full sample rate, after which the sample clock is halted for a programmable time (in 2uS intervals up to 2hours) and then a number of samples are captured at a selected sample rate from the Secondary Channel and/or the Primary Channel. The trigger event is always preserved in sample RAM to allow precise timing of the delayed region. The halted period is deterministic, so the delayed region of data may be referenced to the trigger event accurate to 1 sample. Delay mode may (for example) be used to examine video lines in a frame by triggering on Frame sync and progressivly stepping through delayed traces. Another application may be to examine a region of data in a long repeating cycle.

In addition to the full 25MS/s capture rate (always used initially for trigger search), (D)elayed Trace modes can swap to other sample rates using new slow clock mode or burst mode. These rates begin at 1MHz and extend down to uHz (Super Chop mode). Each mode is available as slow clock or burst mode down to a 4KHz sample rate. Only burst mode is used for the Super Chop mode which can sample slower than 4KHz. If the Burst clock control is used, the sample clock is turned on for 200nS which results in 5 samples being captured at Fs = 25MHz, or 8 samples at Fs = 40MHZ. The new 'A' command can accumulate these sample groups for transmission to the PC.

There are no Delay modes that attempt to impliment a slow clock of greater than 1MHz. Rates above 1MHz may be synthesized by capturing at full sample rate and using 'A' to skip unwanted samples, or sum them to an average (Software TimeBase).

Several Delay modes impliment an interleaved trace, where every 4uS..256uS the primary channel then the secondary channel is sampled. These modes give a dual channel display and are also suitable for implimenting an X-Y display. Up to 8K of data from both channels may be captured. If signals presented to both channels are harmonically related audio signals, an X-Y plot will graphically reveal phase information.

Delay is primarily intended for implimenting DSO and CRO functionality which includes repeating traces. A reliable trigger detect is required for this. To eliminate false triggers due to ADC noise, the Delay command has two optional levels of digital filtering on Trigger detect. The first is a 2uS filter that requires that the Trigger condition generated by SPOCK must consistently be true 3 times in a 2uS window after it is first seen. The second level of trigger filtering is for lower frequency signals. Before TRIG can be seen, a PreTrig filter looks for TRIG to be false for 1...256 uS at 1uS intervals. This is a form of pulse width detection. This filter is controlled by the DFLT0 register. Once this PreTrigger condition is met, either a Pulse Width or a Low Pass integrator is applied to the TRIG TRUE condition to initiate the trace. The TimeConstant/Period of this stage is determined by DFLT1. For low frequency and noisy signals, these filters can discriminate against noise on the TRIG condition. The Pulse detects have a maximum window of 256uS and the LP filter has an effective Time Constant of about 500uS.

(D) Mode has thirteen (13) new registers :-

D_ MODE - byte holds required trace mode
DLY3, DLY2, DLY1, DLY0 - 4 byte delay counter with 2uS intervals
CAP3, CAP2, CAP1,CAP0 - 4 byte capture counter with 2uS intervals
DCNT1 - msb of counter for mode 1-9 bursts
DCNT0 - lsb of counter for mode 1-9 bursts
DFLT0 - Digital Filter variable for PreTrigger condition

DFLT1 - Digital Filter variable for Trigger condition

The D_MODE register uses the high 3 bits to control Trigger Filters -

D_MODE(7) - Activates LF TRIG Filter option
D_MODE(6) - 1 selects LP TRIG Filter, 0 selects PULSE TRIG Filter
D_MODE(5) - Activtes HF 2uS TRIG Filter if (7) is 0

D-Mode 0 - Delayed capture, Fast sample clock
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, the sample clock is restarted and continues for up to 2^32 2uS periods. The clock is halted, and the address counter is read from SPOCK. This is transmitted to the host to terminate the command. The normal range of capture times should be limited to fit within the available sample RAM. The 4 byte value allows for future expansion and is consistent with the delay counter format.
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture time is limited to avoid sample memory wrap around).

D-Mode 1- Delayed Capture, 1MHz Slow Clock
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the Secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Slow Clock mode at a 1MS/s rate. The sampling period is not specified in units of 2uS, but in blocks of 256 samples. The DCNT1 register specifies how many blocks of 256 samples will be captured, resulting in a minimum capture of 256 samples up to 65,536 samples.
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around). In this case, the trigger will be recorded at 25MS/s which is 25 times the resolution of the delayed trace.

D-Mode 2 - Delayed capture, 500KHz Slow Clock
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the Secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Slow Clock mode at a 500KS/s rate. The sampling period is not specified in units of 2uS, but in samples up to 2^16. The DCNT registers specify how many samples will be captured, resulting in a minimum capture of 1 sample up to 65,536

samples .
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around). In this case, the trigger will be recorded at 25MS/s which is 50 times the resolution of the delayed trace.

D-Mode 3 - Delayed Capture, 250KHz Slow Clock, CHOP
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Slow Clock mode at a 250KS/s rate with pairs of alternate samples coming from Primary channel then Secondary channel. The sampling period is not specified in units of 2uS, but in sample pairs up to 2^16. The DCNT registers specify how many sample pairs will be captured, resulting in a minimum capture of 1 sample pair up to 65,536 sample pairs.
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around). In this case, the trigger will be recorded at 25MS/s which is 100 times the resolution of the delayed trace.
To display the interleaved samples, A-Mode 1/2 may be used to dump the primary channel, followed by the secondary channel.

D-Mode 4 - Delayed Capture, Slow Clock Variable Sample Rate 250KHz..4KHz
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Slow Clock mode at a variable sample rate set by VMR_CAP0. The period between samples ranges from 4uS to 259uS in 1uS intervals. The sampling period is not specified in units of 2uS, but in samples up to 2^16. The DCNT registers specify how many samples will be captured, resulting in a minimum capture of 1 sample up to 65,536 samples .
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around).

D-Mode 5 - Delayed Capture, Slow Clock CHOP Variable Sample Rate 200KHz..4KHz
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Slow Clock mode at a variable sample rate set by

VMR_CAP0. The period between samples ranges from 5uS to 260uS in 1uS intervals. The sampling period is not specified in units of 2uS, but in samples up to 2^16. The DCNT registers specify how many samples will be captured, resulting in a minimum capture of 1 sample up to 65,536 samples .
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around).

D-Mode 6- Delayed Capture, 1MHz Burst Clock
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the Secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Burst Clock mode at a 1MHz rate, 5 samples per burst. The sampling period is not specified in units of 2uS, but in blocks of 256 sample bursts. The DCNT1 register specifies how many blocks of 256 sample burstss will be captured, resulting in a minimum capture of 256x5 samples up to 65,536x5 samples.
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around).

D-Mode 7 - Delayed Capture, Burst Clock, Variable Sample Rate 250KHz..4KHz
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted, the secondary channel is selected and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in Burst Clock mode at a variable sample rate set by VMR_CAP0. The period between samples ranges from 4uS to 259uS in 1uS intervals. The sampling period is not specified in units of 2uS, but in sample bursts up to 2^16. The DCNT registers specify how many sample bursts will be captured, resulting in a minimum capture of 1x5 samples up to 65,536x5 samples .
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around).

D-Mode 8 - Delayed Capture, Burst Clock, CHOP Variable Sample Rate 250KHz..4KHz
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted and a delay of up to 2^32 2uS periods begins. At the end of this delay, sampling resumes in burst mode. The burst is 3 PIC cycles long, with the second cycle allowing time for the MUX to swap from Primary Channel to Secondary channel. Given a 200nS PIC cycle (20MHz) and 25MHz sample clock, the burst sequence will capture 15 samples - including

primary and secondary channels.The period between samples ranges from 4uS to 259uS in 1uS intervals. The sampling period is not specified in units of 2uS, but in sample bursts up to 2^16. The DCNT registers specify how many sample bursts will be captured, resulting in a minimum capture of 1x15 samples up to 65,536x15 samples .
Note that this trace mode will always retain the section of waveform which activated the trigger (providing that the subsequent capture is limited to avoid sample memory wrap around).

D-Mode 9 - Delayed Capture, Burst Clock CHOP Variable Sample Rate, 125KHz ..116uHz
This versatile mode allows both channels to be burst sampled after the delay period with a subsequent (n x 2uS) period between bursts. The 32 bit CAP registers are used to specify the intersample delay. This gives Mode 9 (Super Chop) a huge range of sample rates with fine control over the sample period. The burst is 3 PIC cycles long, with the second cycle allowing time for the MUX to swap from Primary Channel to Secondary channel. Given a 200nS PIC cycle (20MHz) and 25MHz sample clock, the burst sequence will capture 15 samples - including primary and secondary channels.
The sample clock is turned on and Trigger is searched on the Primary channel. When trigger is found the sample clock is halted and a delay of up to 2^32 2uS periods begins. At the end of this delay, a dual channel burst of samples starts and is padded to 4uS. A subsequent delay of 1 up to 2^32 2uS ticks begins. This burst sequence is repeated DCNT times. To display the interleaved samples, A-Mode 1/2/3 may be used to extract the primary channel, followed by the secondary channel.

D-Mode 16..25 Modified Delayed trace with continuous clock
The D-Mode byte, (bit 4) being set modifies the way the above modes work by preventing the sample clock from being halted after trigger is found. This means continuous traces through the delay period, when the sample method switches to the specified mode.
This bit may be used with mode 0 to give an effective ALT mode of sampling. Trace with the SEC channel set the same as the PRIM to get the PRIM channel, then retrace with the SEC channel swapping after trigger. If the PRIM trigger points match, then the alternate traces may be overlayed. Also, the time calculations are simpler that the old Trace modes.

(L)ogic Mode Trace command

This is a new Trace mode command that is especially effective for Logic Analyzer operation, although it may also be used for Analog and mixed mode captures. This mode covers the sample rates from 25MHz down to 4KHz. The PRIMARY analog channel is selected as default, and swapped to the secondary

after TRIG. Upon initiating this trace, the whole of sample RAM is filled at the selected sample rate to guarantee pretrigger data . Next, 'L' triggers at the selected sample rate, after which the sampling continues for up to 64K samples as specified in the CAP,DCNT registers (shared with (D)elay mode). By specifying the number of sample points collected after TRIG, the available Sample RAM may be divided between PRE-TRIG and POST-TRIG data in an arbitrary way.
The recommended trigger setup for 'L' is positive edge triggered Logic source. This is effective with slow clock mode with SPOCK monitoring the Logic Bus. The ZZ-CLK signal is pulsed low for 200uS and remains high for the rest of the time. This means the Logic buffer (573 device) always passes data to SPOCK, and SPOCK will trigger the PIC if the programmed trigger conditions are met - even if the trigger happens between sample points. This feature means that it will be possible to trigger on a transient logic event which may not be recorded in the sample record at the rate selected.

(L)ogic Trace has 8 registers associated with it

L_MODE - selects the Logic Trace mode
DLY1 - hi byte of delay counter (shared with Delay)
DLY0 - lo byte of delay counter (shared with Delay)
CAP1 - hi byte of capture counter (shared with Delay)
CAP0 - lo byte of capture counter (shared with Delay)
DCOUNT1 - hi byte of sample count (shared with Delay)
DCOUNT0 - lo byte of sample count (shared with Delay)
L_RATE - byte variable determines the sample period of Mode 4

L-Mode 0 - Logic trace at HW Sample rate (25MHz)
This mode impliments a Logic capture at 25MS/s. The buffer is filled with CAP0,1 periods of 2uS data before looking for trigger condition. After TRIG is seen, CAP0,1 periods of 2uS are collected.

L-Mode 1 - Logic trace at 1MHz
This mode impliments a Logic capture at 1MS/s. The buffer is filled before looking for trigger condition. After TRIG is seen, DCOUNT1 blocks of 256 samples are collected.

L-Mode 4 - Logic trace at Variable rate 250KHz..4KHz
This mode impliments a Logic capture at a variable sample rate of 250KS/s down to 4KS/s. The buffer is filled before looking for trigger condition. After TRIG is seen, DCOUNT samples are collected.
The sample rate is determined by Period = (3 + L_RATE) uS.
L_RATE =1 gives 250KS/s
L_RATE = 17 gives 50KS/s
L_RATE = 97 gives 10KS/s
L_RATE = 247 gives 4KS/s

(L)ogic trace provides a very simple way of implimenting a Logic Analyser with

Bitscope. Capturing at full sample rate has been well covered, but previously it was not possible to collect an arbitrary number of pretrigger samples at a wide range of sample rates. L-Mode 0 captures at full sample rate and uses the simple 2uS period register (shared with D Mode0). The buffer is prefilled, so an arbitrary trigger position (to 2uS) in the buffer is possible. L-Mode 1 captures at 1MS/s, and L-Mode 4 can now capture from 250KHz down to 4KS/s, which covers a 4 second window. To maximise the utility of the Logic modes, the analog capture swaps to SEC channel when trigger is seen. This allows 2 alalog sources to be seen in one trace.